Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus comprising:

a queue storing a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks~~, the memory bus incapable of transmitting the plurality of memory transactions simultaneously~~; and

an arbiter coupled to each of the plurality of memory transactions and configured to

~~identify~~ generate a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction, and

select one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

2. (original) The apparatus of claim 1, further comprising:

a memory controller configured to send the selected memory transaction over the memory bus.

3. (original) The apparatus of claim 1, further comprising:

a queue controller configured to associate with each of the memory transactions a different priority in a set of priorities; and wherein

the arbiter is further configured to select the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

4. (original) The apparatus of claim 3, wherein:

each priority represents an age of a memory transaction.

5. (currently amended) The apparatus of claim 1, wherein:

~~the arbiter is further configured to generate the bank readiness signals~~ the plurality of memory transactions enter the queue at a first request station and progress toward a second request station until selected for transmission over the memory bus based on the bank readiness signals.

6. (original) The apparatus of claim 1, wherein:

the arbiter is further configured to send a memory transaction to a memory bank, clear the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank, and set the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

7. (currently amended) A method comprising:

identifying a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks~~, the memory bus incapable of transmitting the plurality of memory transactions simultaneously~~;

~~identifying~~ generating a plurality of bank readiness signals by monitoring the memory bus, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

selecting one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

8. (original) The method of claim 7, further comprising:

sending the selected memory transaction over the memory bus.

9. (original) The method of claim 7, wherein each of the memory transactions is associated with a different priority in a set of priorities, and wherein selecting further comprises:

selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

10. (original) The method of claim 9, further comprising:

associating the priorities with the memory transactions based on an age of the memory transactions.

11. (currently amended) The method of claim 7, ~~further comprising~~ wherein generating comprises:

generating the bank readiness signals using a state machine coupled to the memory bus.

12. (original) The method of claim 7, wherein generating comprises:

sending a memory transaction to a memory bank;

clearing the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank; and

setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

13. (currently amended) An apparatus comprising:

means for identifying a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks~~, the memory bus incapable of transmitting the plurality of memory transactions simultaneously~~;

means for ~~identifying~~ generating a plurality of bank readiness signals based upon a content of the memory bus, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

means for selecting one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

14. (original) The apparatus of claim 13, further comprising:

means for sending the selected memory transaction over the memory bus.

15. (original) The apparatus of claim 13, wherein each of the memory transactions is associated with a different priority in a set of priorities, and wherein means for selecting further comprises:

means for selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

16. (original) The apparatus of claim 15, further comprising:

means for associating the priorities with the memory transactions based on an age of the memory transactions.

17. (currently amended) The apparatus of claim 13, ~~further comprising:~~

~~means for generating the bank readiness signals~~ wherein the content of the memory bus comprises an address of a memory transaction monitored by a state machine.

18. (original) The apparatus of claim 13, wherein means for generating comprises:

means for sending a memory transaction to a memory bank;

means for clearing the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank; and

means for setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

19. (currently amended) A computer program product, tangibly stored on a computer-readable medium, the product comprising instructions operable to cause a programmable processor to:

identify a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks~~, the memory bus incapable of transmitting the plurality of memory transactions simultaneously~~;

~~identify~~ generate a plurality of bank readiness signals based upon a content of the memory bus, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

select one of the memory transactions for transmission over the memory bus based on the bank readiness signals.

20. (new) The apparatus of claim 13, wherein the plurality of memory transactions are sent over the memory bus one memory transaction at a time.

21. (new) An apparatus comprising:

a memory bus capable of transmitting N memory transaction items at a time;

a queue capable of storing more than N memory transaction items;

a memory circuit coupled to the memory bus;

a multiplexer comprising at least N multiplexer inputs and a multiplexer output, wherein each multiplexer input is coupled to one of the memory transaction items and wherein the multiplexer output is coupled to the memory bus;

a state machine coupled to the multiplexer output; and

an arbiter controller coupled to the state machine and a selection input of the multiplexer.

22. (new) An apparatus comprising:

a queue circuit comprising a plurality of stations, each station coupled to a memory transaction request line;

a memory transaction multiplexer circuit comprising a plurality of multiplexer inputs, a multiplexer output, and a multiplexer selection input, each multiplexer input coupled to one of the memory transaction request lines; and

a memory circuit, coupled to the multiplexer output.

23. (new) The apparatus of claim 22 further comprising:

a state machine circuit comprising a state machine input and a state machine output, wherein the state machine input is coupled to the multiplexer output, and the state machine output is coupled to a selection input of the memory transaction multiplexer circuit.

24. (new) The apparatus of claim 22 further comprising:

a state machine comprising a state machine input coupled to the multiplexer output and a plurality of state machine outputs; and

an arbiter controller comprising a plurality of arbiter inputs and an arbiter output, wherein each of the plurality of arbiter inputs is coupled to one of the plurality of state machine outputs. and the arbiter output is coupled to the multiplexer selection input.

25. (new) The computer program product of claim 19, wherein the content of the memory bus comprises an address of a memory transaction monitored by a state machine.